| Notice of Allowability | Application No. | Applicant(s) | |
|---|---|---|---|
| | 10/767,069 | SHUKURI, SHOJI | |
| | Examiner | Art Unit | |
| | David Nhu | 2818 | |

*-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address--*

All claims being allowable, PROSECUTION ON THE MERITS IS (OR REMAINS) CLOSED in this application. If not included herewith (or previously mailed), a Notice of Allowance (PTOL-85) or other appropriate communication will be mailed in due course. **THIS NOTICE OF ALLOWABILITY IS NOT A GRANT OF PATENT RIGHTS.** This application is subject to withdrawal from issue at the initiative of the Office or upon petition by the applicant. See 37 CFR 1.313 and MPEP 1308.

1. ☒ This communication is responsive to *7/7/05*.

2. ☒ The allowed claim(s) is/are *52-57,63-67,71-74 and 86-150*.

3. ☒ The drawings filed on *30 January 2004* are accepted by the Examiner.

4. ☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
   a) ☒ All b) ☐ Some* c) ☐ None of the:
      1. ☒ Certified copies of the priority documents have been received.
      2. ☒ Certified copies of the priority documents have been received in Application No. *10/400,469* .
      3. ☐ Copies of the certified copies of the priority documents have been received in this national stage application from the International Bureau (PCT Rule 17.2(a)).

   * Certified copies not received: _____.

Applicant has THREE MONTHS FROM THE "MAILING DATE" of this communication to file a reply complying with the requirements noted below. Failure to timely comply will result in ABANDONMENT of this application.
**THIS THREE-MONTH PERIOD IS NOT EXTENDABLE.**

5. ☐ A SUBSTITUTE OATH OR DECLARATION must be submitted. Note the attached EXAMINER'S AMENDMENT or NOTICE OF INFORMAL PATENT APPLICATION (PTO-152) which gives reason(s) why the oath or declaration is deficient.

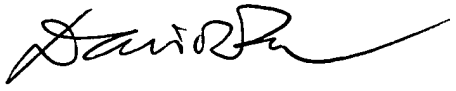
6. ☐ CORRECTED DRAWINGS ( as "replacement sheets") must be submitted.
   (a) ☐ including changes required by the Notice of Draftsperson's Patent Drawing Review ( PTO-948) attached
      1) ☐ hereto or 2) ☐ to Paper No./Mail Date _____.
   (b) ☐ including changes required by the attached Examiner's Amendment / Comment or in the Office action of Paper No./Mail Date _____.

   **Identifying indicia such as the application number (see 37 CFR 1.84(c)) should be written on the drawings in the front (not the back) of each sheet. Replacement sheet(s) should be labeled as such in the header according to 37 CFR 1.121(d).**

7. ☐ DEPOSIT OF and/or INFORMATION about the deposit of BIOLOGICAL MATERIAL must be submitted. Note the attached Examiner's comment regarding REQUIREMENT FOR THE DEPOSIT OF BIOLOGICAL MATERIAL.

**Attachment(s)**

1. ☐ Notice of References Cited (PTO-892)
2. ☐ Notice of Draftperson's Patent Drawing Review (PTO-948)
3. ☐ Information Disclosure Statements (PTO-1449 or PTO/SB/08), Paper No./Mail Date _____
4. ☐ Examiner's Comment Regarding Requirement for Deposit of Biological Material
5. ☐ Notice of Informal Patent Application (PTO-152)
6. ☐ Interview Summary (PTO-413), Paper No./Mail Date _____.
7. ☐ Examiner's Amendment/Comment
8. ☒ Examiner's Statement of Reasons for Allowance
9. ☐ Other _____.



## REASONS FOR ALLOWANCE

1. Claims 52-57, 63-67, 71-74, 86-150 are allowed.

2. The following is an examiner's statement of reasons for allowance: None of the references of record teaches or suggests as cited in claims 52, 63, 71, 87, 89, 91, 98, 101, 104, 105, 110, 113, 123, 127, 131, 135 : patterning said first conductive film in said memory cell forming region to form a first conductor pattern which serves as a first gate electrode of a memory cell; forming a second conductive film over said memory cell forming region and over said first conductive film in said peripheral circuit forming region; etching said second conductive film to form a second gate electrode of said memory cell on at least side surface of said conductor pattern, and to form an electrode structure of a peripheral circuit element comprising said circuit forming region; forming a first silicide layer on said first gate electrode of said memory cell and a second silicide layer on said second gate electrode of said memory cell (as cited in claims 52); etching said insulating film and said first conductive film to form a first conductor pattern which serves as a first gate electrode of a memory cell; forming a second gate electrode of said memory cell on side walls of said first conductor film; removing said insulating film over said first conductor pattern; forming sidewall spacers, each comprised of an insulating film, in self-alignment with side walls of said second gate electrode; forming a silicide layer for each of said first conductor pattern and said second gate electrode in self-alignment with respect to said sidewalls spacers to form corresponding first electrode (as cited in claims 63, 71); forming an insulator film over side said memory of said first conductor pattern and over said memory cell forming region; forming a second conductive film over said memory cell forming region and said insulator film; etching said second conductive film to form a second

gate electrode of said memory cell on at least side surface of said first conductor pattern; forming a sidewall spacers of an insulator material in self-alignment with side walls of said second gate electrode; forming a first silicide layer on said second gate electrode of said memory cell, wherein said first silicide layer and said second silicide layer are electrically separated (as cited in claim 87); forming an insulator film over side said memory of said first conductor pattern and over said memory cell forming region; forming a second conductive film over said memory cell forming region and said insulator film; etching said second conductive film to form a second conductor pattern in self-alignment with said surface of said first conductor pattern such that said second conductor pattern has a shape of a sidewall spacer; removing said second conductor pattern to form a second gate electrode of said memory cell on side of said side surfaces of said first conductor pattern; forming sidewall spacers of an insulator material in self-alignment with side walls of said second gate electrode and in self-alignment with said side surfaces of said first gate electrode; forming a first silicide layer on said first gate electrode of said memory cell and a second silicide layer on said second gate electrode and said memory cell, wherein said first silicide layer and said second silicide layer are electrically separated (as cited in claims 89, 91, 123); forming a second gate electrode of said memory cell in self-alignment with said side surface of said first conductor pattern such that said second gate electrode has a shape of a sidewall spacer and such that said insulator film is formed between said first conductor pattern and said second gate electrode; forming a first silicide layer on said first gate electrode of said memory cell and a second silicide layer on said second gate electrode of said memory cell; wherein said first silicide layer and said second silicide layer are electrically separated (as cited in claims 98, 110); selectively forming

a second gate electrode of said memory cell in self-alignment with one side surface of said first conductor pattern such that said second gate electrode gas a shape of a sidewall spacer and such that said insulator film is formed between said first conductor pattern and said second gate electrode; forming sidewall spacers of an insulator material in self-alignment with side walls of said second gate electrode, in self-alignment with other side surface of said first conductor pattern; forming a first silicide layer on said first gate electrode of said memory cell and a second silicide layer on said second gate electrode and said memory cell, wherein said first silicide layer and said second silicide layer are electrically separated (as cited in claims 101); forming a second gate electrode of said memory cell in self-alignment with said side surface of said first conductor pattern such that said second gate electrode has a shape of a sidewall spacer and such that said insulator film is formed between said first conductor pattern and said second gate electrode; forming a gate electrode of a peripheral circuit transistor by patterning said first conductive film in said peripheral circuit forming region; forming sidewall spacers of an insulator material in self-alignment with side walls of said second gate electrode, in self-alignment with said side surface of said first gate electrode and in self-alignment with side surfaces of said gate electrode of said peripheral circuit transistor; forming a first silicide layer on said first gate electrode of said memory cell and a second silicide layer on said second gate electrode and said memory cell and a third silicide layer on said gate electrode of said peripheral circuit transistor, wherein said first silicide layer and said second silicide layer are electrically separated (as cited in claims 104, 127, 131); selectively forming a second gate electrode of said memory cell in self-alignment with one side surface of said first conductor pattern such that said second gate electrode gas a shape of a sidewall spacer and such that

said insulator film is formed between said first conductor pattern and said second gate electrode; forming a gate electrode of a peripheral circuit transistor by patterning said first conductive film in said peripheral circuit forming region; forming sidewall spacers of an insulator material in self-alignment with side walls of said second gate electrode, in self-alignment with other side surface of said first conductor pattern, and in self-alignment with side surfaces of said gate electrode of said peripheral circuit transistor; wherein said first silicide layer and forming a first silicide layer on said first gate electrode of said memory cell, a second silicide layer on said second gate electrode of said memory cell and a third silicide layer on said gate electrode of said peripheral circuit transistor; said second silicide layer are electrically seaparated ( as cited in claim 105); forming a first silicide layer on said first gate electrode of said memory cell and a second silicide layer on said second gate electrode and said memory cell, wherein said first silicide layer and said second silicide layer are electrically separated (as cited in claims 101);forming an insulator film over side said memory of said first conductor pattern and over said memory cell forming region; forming a second conductive film over said memory cell forming region and said insulator film; etching said second conductive film to form a second conductor pattern in self-alignment with said surface of said first conductor pattern such that said second conductor pattern has a shape of a sidewall spacer; removing said second conductor pattern to form a second gate electrode of said memory cell on side of said side surfaces of said first conductor pattern; forming sidewall spacers of an insulator material in self-alignment with side walls of said second gate electrode and in self-alignment with said side surfaces of said first gate electrode; forming a first silicide layer on said first gate electrode of said memory cell and a second silicide layer on said second gate electrode and said

memory cell, wherein a height of said first gate electrode is different from a height of said second gate electrode, and wherein said first silicide layer and said second silicide layer are electrically separated (as cited in claims 113); forming a second gate electrode of said memory cell in self-alignment with said side surface of said first gate electrode such that said second gate electrode has a shape of a sidewall spacer and such that said insulator film is formed between said first gate electrode and said second electrode, wherein said second gate electrode forming step, a third conductor pattern is formed over said second conductor pattern; and forming a first silicide layer on said first gate electrode of said memory cell and a second silicide layer on said second gate electrode and said memory cell, wherein said first silicide layer and said second silicide layer are electrically separated (as cited in claims 135).

3. Any comments considered necessary by applicant must be submitted no later than the payment of the issue fee and, to avoid processing delays, should preferably accompany the issue fee. Such submissions should be clearly labeled "Comments on Statement of Reasons for Allowance."

**CONCLUSION**

4. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure: Shimizu et al (6,555,427 B1): Non-Volatile Semiconductor Memory Device and Manufacturing Method Thereof.

5. Any inquiry concerning this communication on earlier communications from the examiner should be directed to David Nhu , (571)272-1792. The examiner can normally be reached on Monday-Friday from 7:30 AM to 5:00 PM.

The examiner's supervisor, David Nelms can be reached on (571)272-1787.

*The fax phone number for the organization where this application or proceeding is assigned is (703) 872-9306.*

*Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is (703) 308-0956*

David Nhu

July 19, 2005

DAVID NHU
PRIMARY EX